FIG. 1

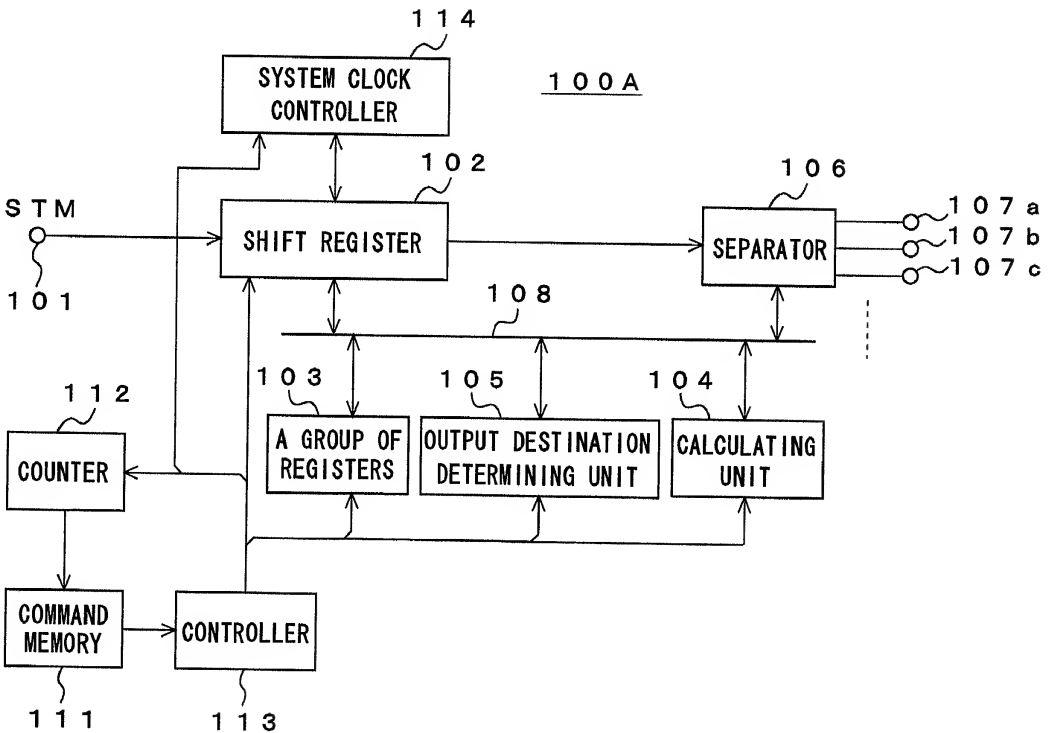

114
SYSTEM CLOCK CONTROLLER
100A
102
106
STM
101
SHIFT REGISTER
SEPARATOR
107a
107b
107c
108
103
105
104
112
A GROUP OF REGISTERS
OUTPUT DESTINATION DETERMINING UNIT
CALCULATING UNIT
COUNTER
COMMAND MEMORY
CONTROLLER
111
113

FIG. 2

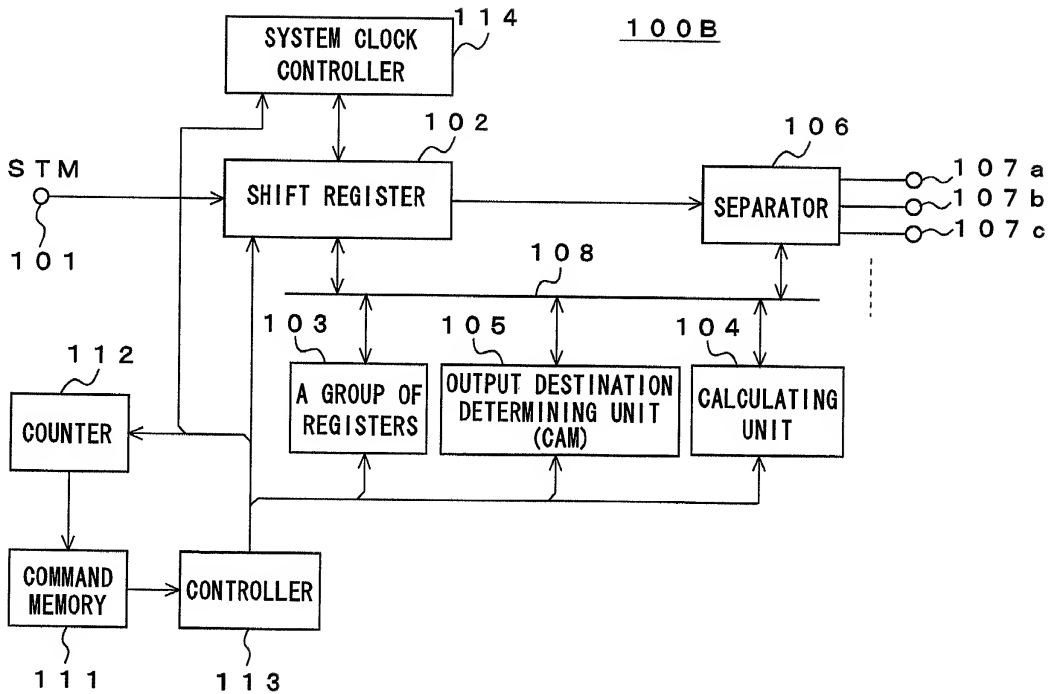

SYSTEM CLOCK CONTROLLER
114
100B
102
106
STM
SHIFT REGISTER
SEPARATOR
107a
107b
107c
101
108
103
105
104
112
A GROUP OF REGISTERS
OUTPUT DESTINATION DETERMINING UNIT (CAM)
CALCULATING UNIT
COUNTER
COMMAND MEMORY
CONTROLLER
111
113

FIG. 3

PACKET ID 0	CONTINUITY COUNT 0	DESTINATION 0
PACKET ID 1	CONTINUITY COUNT 1	DESTINATION 1
PACKET ID 2	CONTINUITY COUNT 2	DESTINATION 2
PACKET ID 3	CONTINUITY COUNT 3	DESTINATION 3
⋮	⋮	⋮

FIG. 9

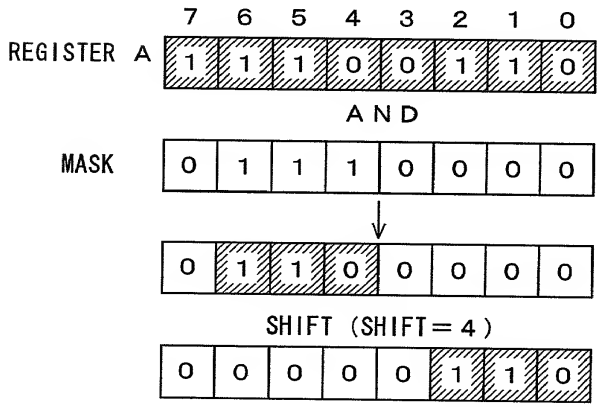
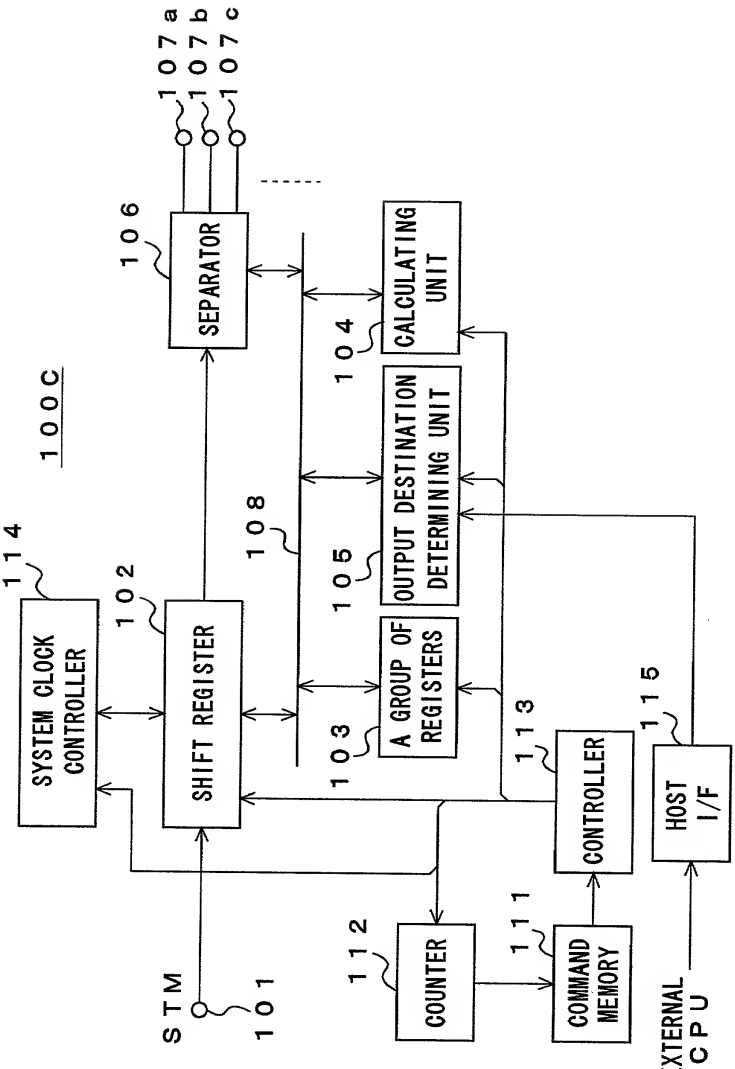


FIG. 4


100c
SYSTEM CLOCK CONTROLLER
114
SHIFT REGISTER
102
SEPARATOR
106
107a
107b
107c
108
A GROUP OF REGISTERS
103
OUTPUT DESTINATION DETERMINING UNIT
105
CALCULATING UNIT
104
CONTROLLER
113
HOST I/F
115
COUNTER
112
COMMAND MEMORY
111
STM
101
EXTERNAL CPU

PRESENT STANDARD

FIG. 5

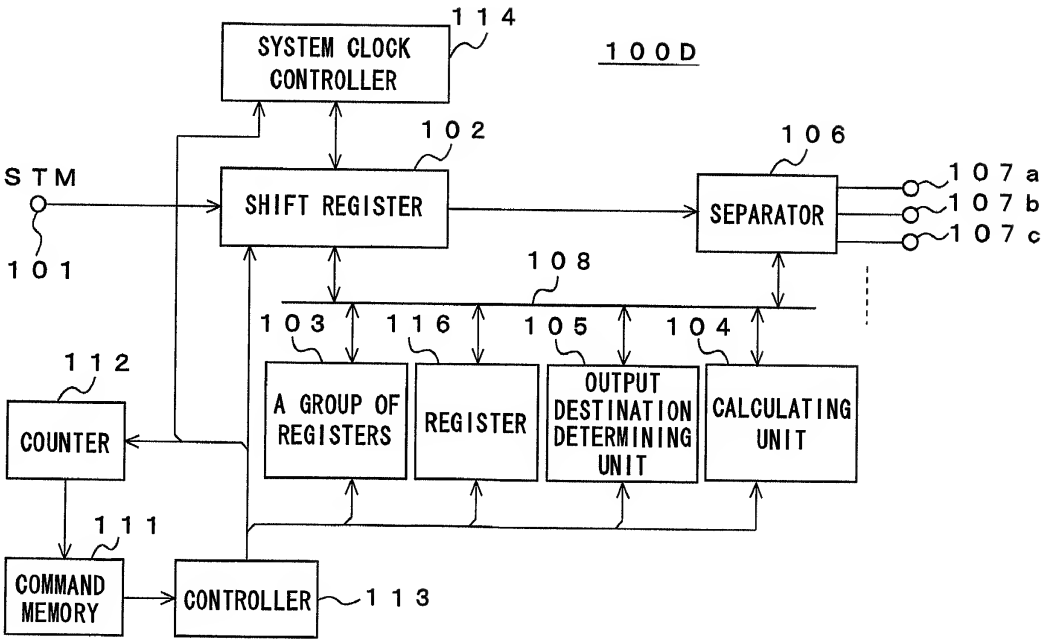
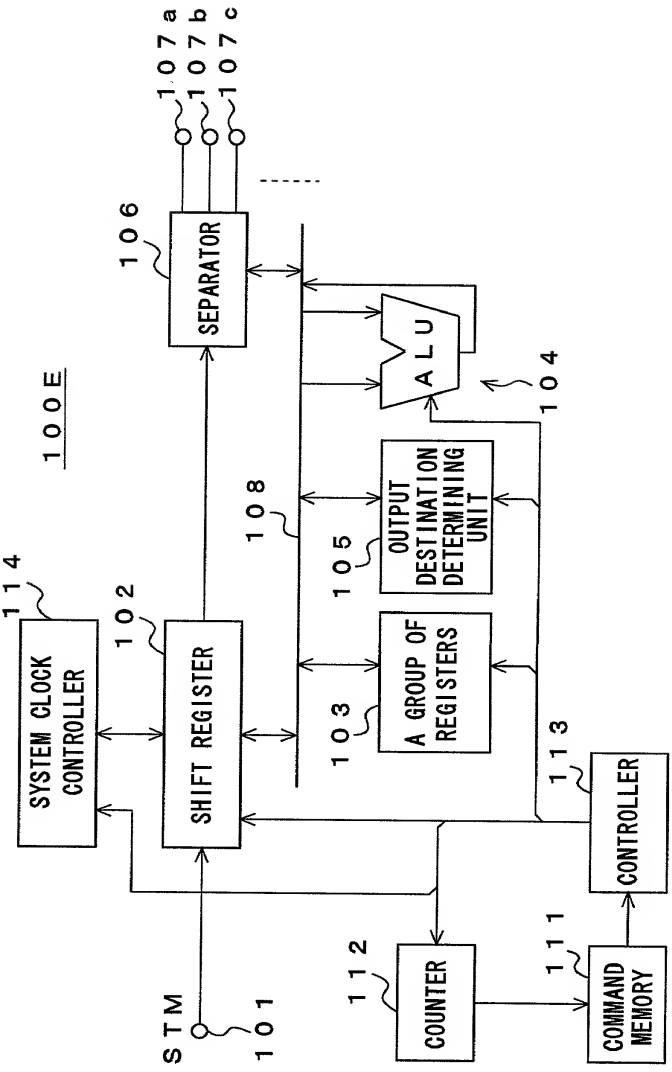


FIG. 6


100E
SYSTEM CLOCK CONTROLLER
114
SHIFT REGISTER
102
STM
101
SEPARATOR
106
107a
107b
107c
108
A GROUP OF REGISTERS
103
OUTPUT DESTINATION DETERMINING UNIT
105
ALU
104
CONTROLLER
113
COUNTER
112
COMMAND MEMORY
111

FASEB' 8Tb0h850

FIG. 7

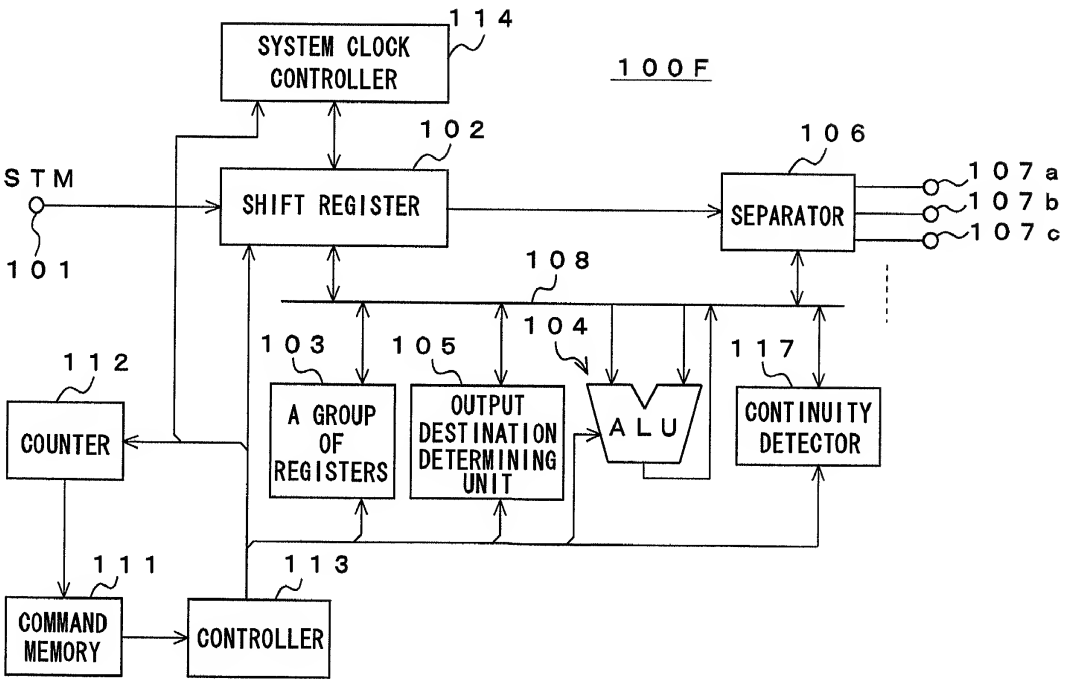


FIG. 8

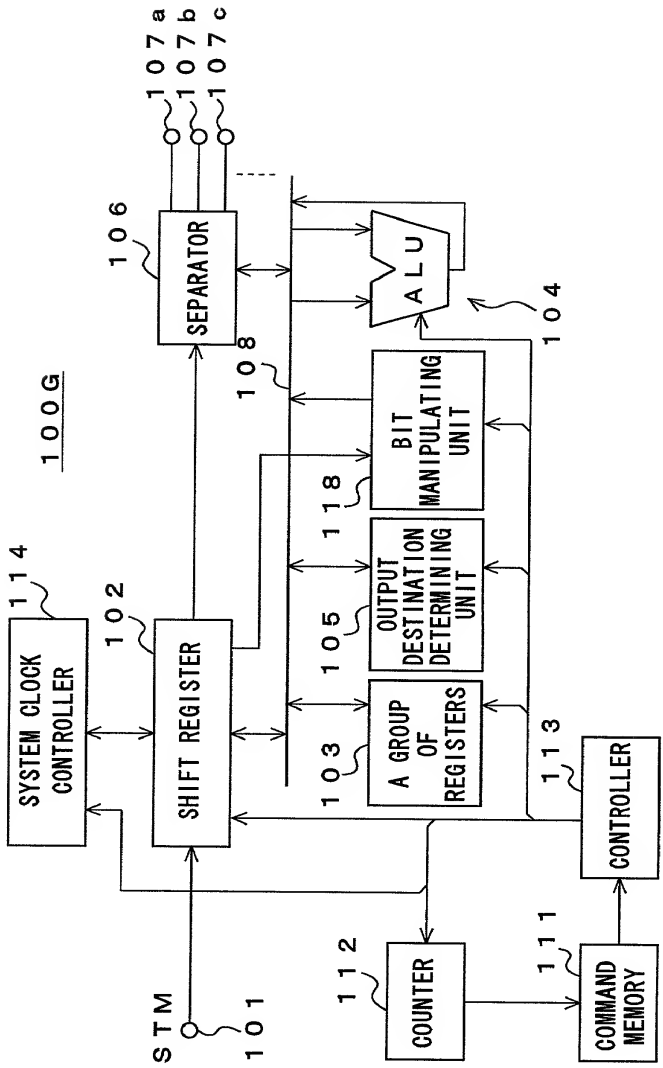

100G
SYSTEM CLOCK CONTROLLER
114
SHIFT REGISTER
102
SEPARATOR
106
107a
107b
107c
108
ALU
104
BIT MANIPULATING UNIT
118
OUTPUT DESTINATION DETERMINING UNIT
105
A GROUP OF REGISTERS
103
CONTROLLER
113
STM
101
COUNTER
112
COMMAND MEMORY
111

FIG. 10

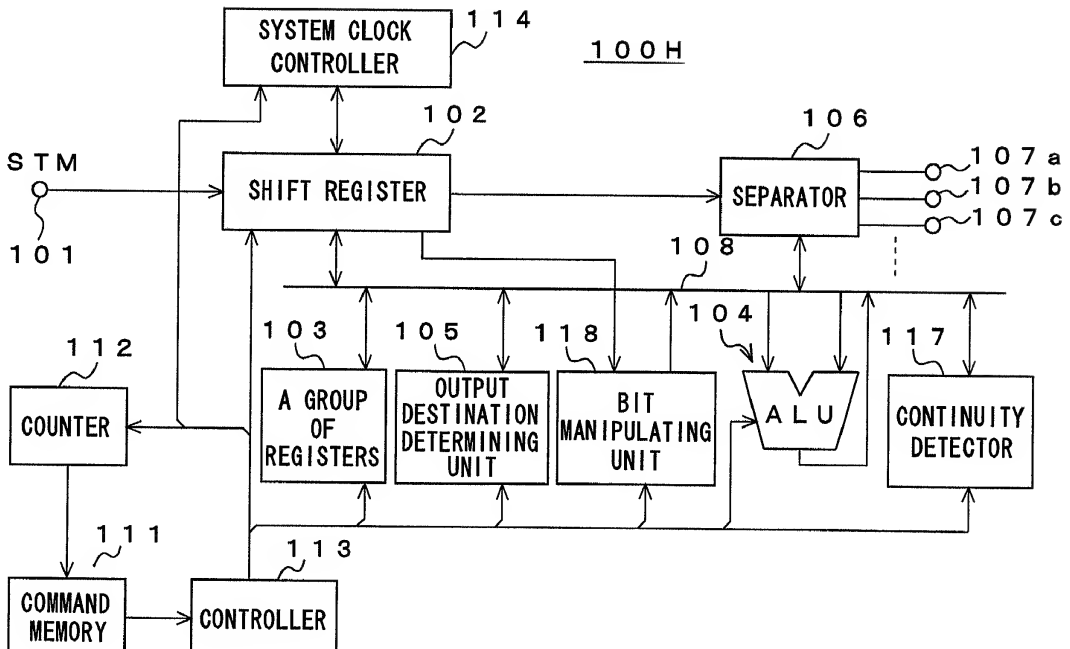

SYSTEM CLOCK CONTROLLER
114
100H
102
106
STM
101
SHIFT REGISTER
SEPARATOR
107a
107b
107c
108
104
103
105
118
117
112
A GROUP OF REGISTERS
OUTPUT DESTINATION DETERMINING UNIT
BIT MANIPULATING UNIT
ALU
CONTINUITY DETECTOR
COUNTER
111
113
COMMAND MEMORY
CONTROLLER

FIG. 11

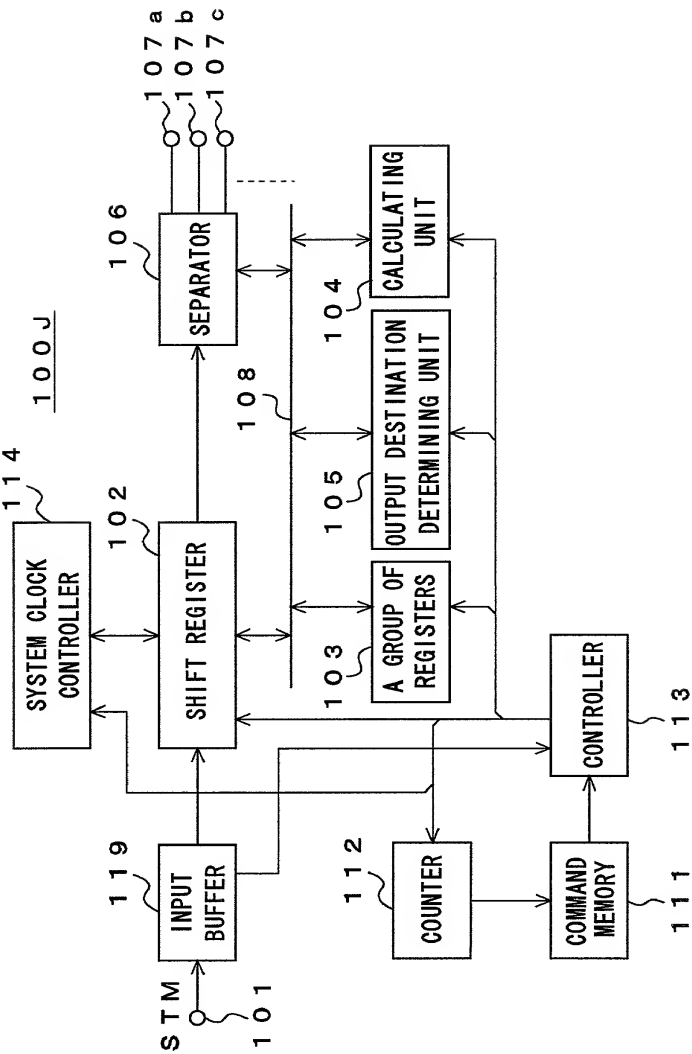

100J
STM
101
INPUT BUFFER
119
SHIFT REGISTER
102
SYSTEM CLOCK CONTROLLER
114
SEPARATOR
106
107a
107b
107c
108
A GROUP OF REGISTERS
103
OUTPUT DESTINATION DETERMINING UNIT
105
CALCULATING UNIT
104
COUNTER
112
COMMAND MEMORY
111
CONTROLLER
113

FIG. 12

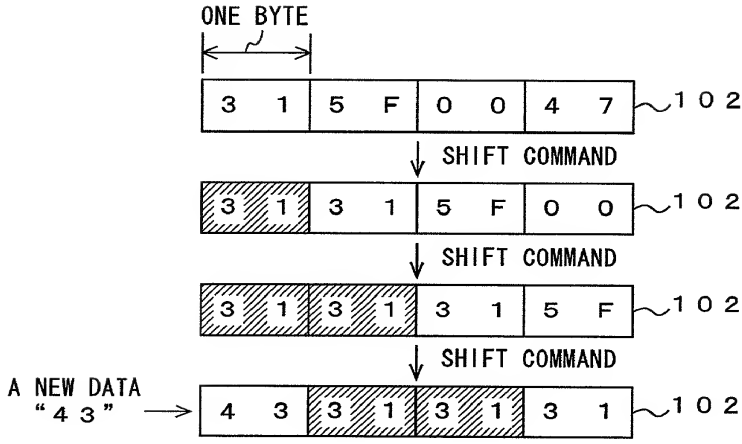

ONE BYTE
3 1 5 F 0 0 4 7
102
SHIFT COMMAND
3 1 3 1 5 F 0 0
102
SHIFT COMMAND
3 1 3 1 3 1 5 F
102
SHIFT COMMAND
A NEW DATA
"43"
4 3 3 1 3 1 3 1
102

FIG. 14

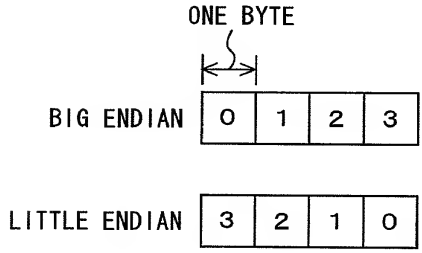
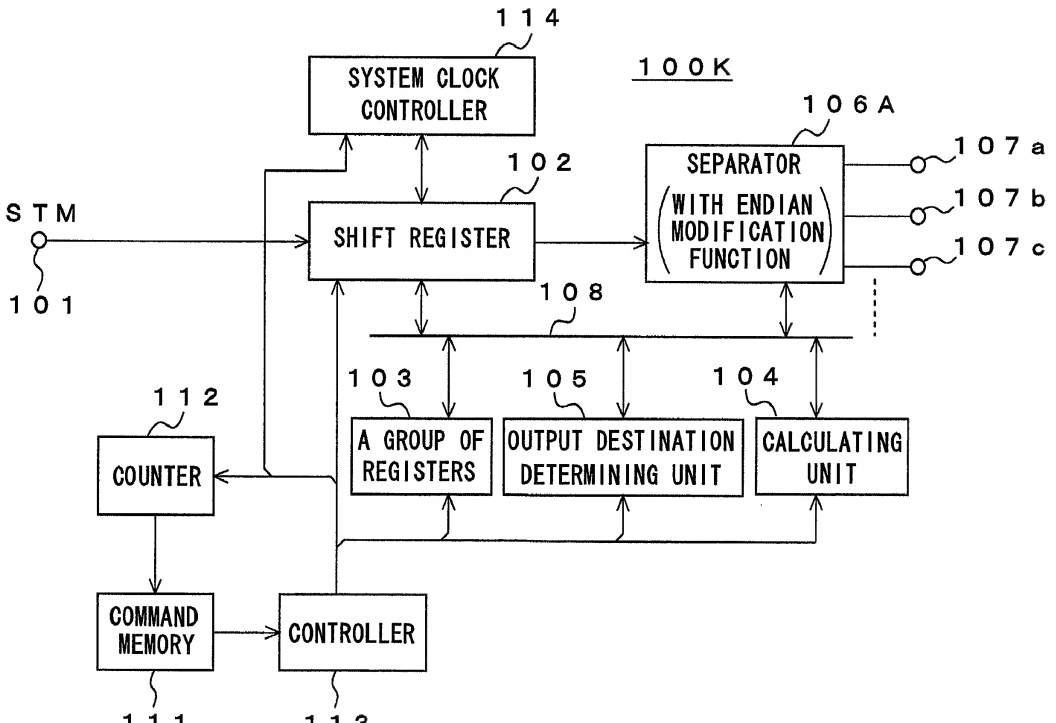

ONE BYTE
BIG ENDIAN
0 1 2 3
LITTLE ENDIAN
3 2 1 0

FIG. 13


114
SYSTEM CLOCK CONTROLLER
100K
106A
SEPARATOR (WITH ENDIAN MODIFICATION FUNCTION)
107a
107b
107c
102
STM
101
SHIFT REGISTER
108
103
105
104
112
A GROUP OF REGISTERS
OUTPUT DESTINATION DETERMINING UNIT
CALCULATING UNIT
COUNTER
COMMAND MEMORY
CONTROLLER
111
113

PUBLISHED APPLICATION

FIG. 15

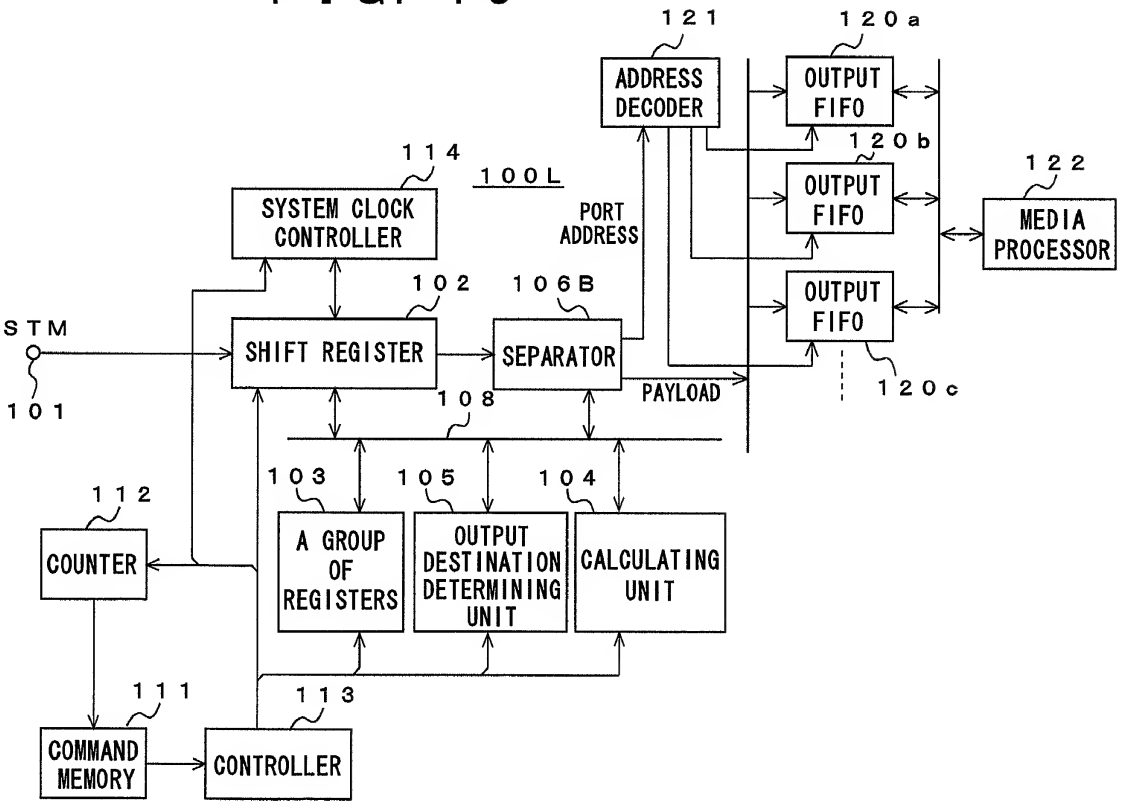


FIG. 16

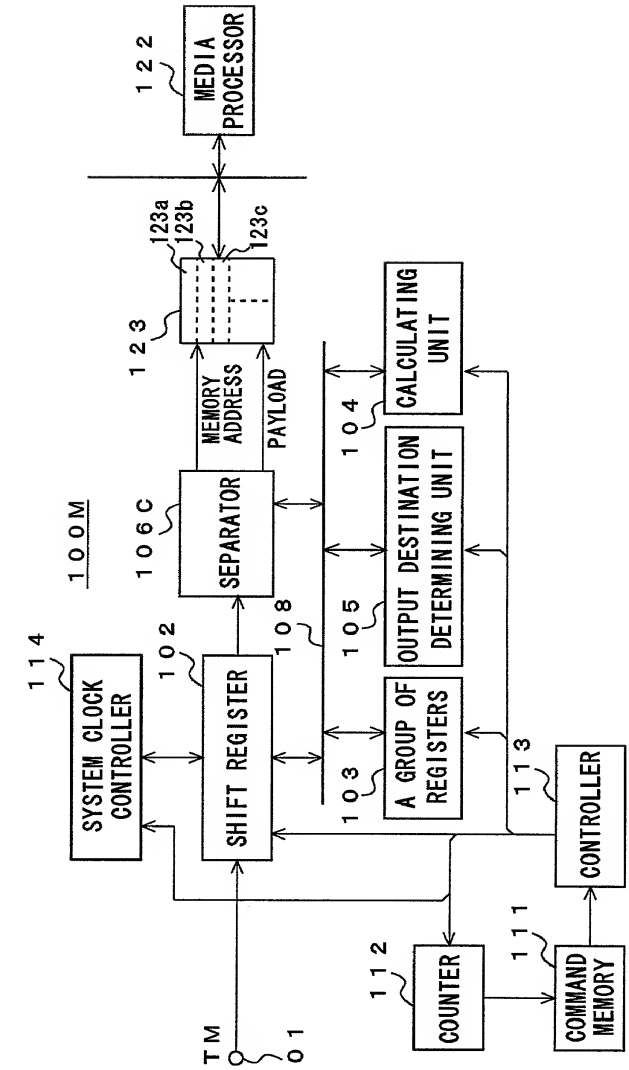

STM
101
SYSTEM CLOCK CONTROLLER
114
SHIFT REGISTER
102
100M
SEPARATOR
106C
MEMORY ADDRESS
PAYLOAD
123
123a
123b
123c
MEDIA PROCESSOR
122
108
105
OUTPUT DESTINATION DETERMINING UNIT
104
CALCULATING UNIT
103
A GROUP OF REGISTERS
113
CONTROLLER
COUNTER
112
111
COMMAND MEMORY

FIG. 17

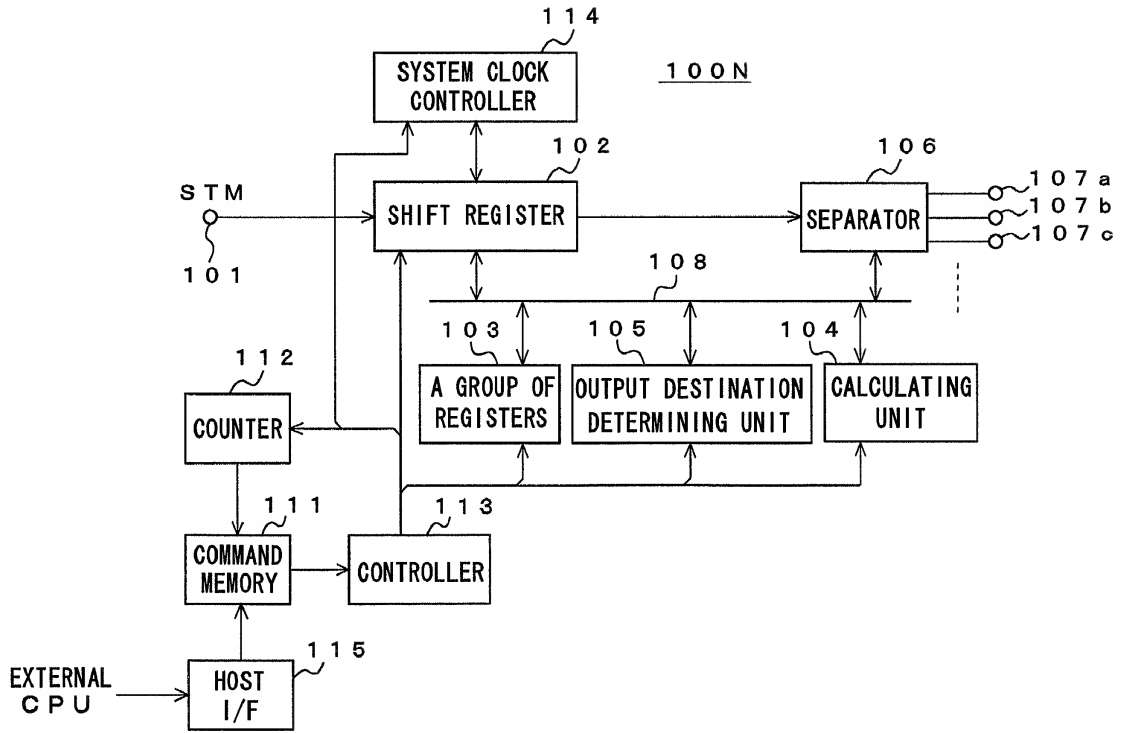

114
SYSTEM CLOCK CONTROLLER
100N
102
106
STM
101
SHIFT REGISTER
SEPARATOR
107a
107b
107c
108
103
105
104
112
A GROUP OF REGISTERS
OUTPUT DESTINATION DETERMINING UNIT
CALCULATING UNIT
COUNTER
111
113
COMMAND MEMORY
CONTROLLER
115
EXTERNAL CPU
HOST I/F

FIG. 18

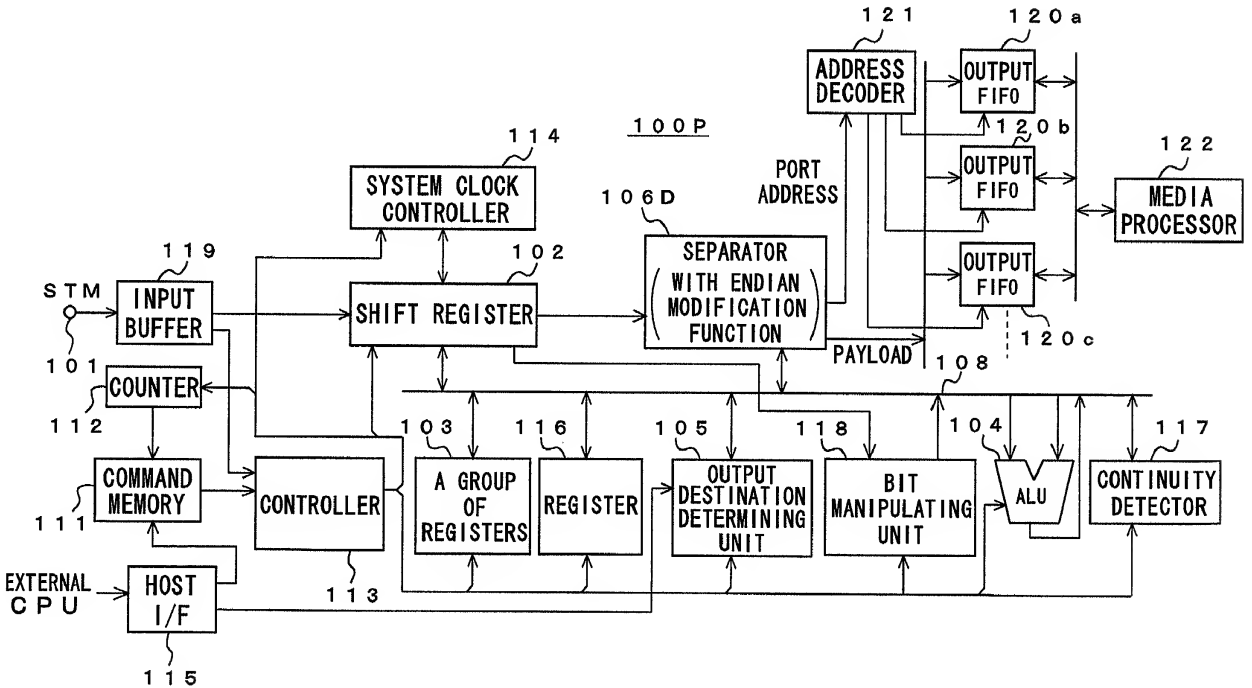

121
120a
ADDRESS DECODER
OUTPUT FIFO
120b
OUTPUT FIFO
122
MEDIA PROCESSOR
OUTPUT FIFO
120c
100P
114
SYSTEM CLOCK CONTROLLER
106D
PORT ADDRESS
SEPARATOR (WITH ENDIAN MODIFICATION FUNCTION)
PAYLOAD
119
STM
INPUT BUFFER
102
SHIFT REGISTER
101
COUNTER
112
108
103
116
105
118
104
117
COMMAND MEMORY
111
CONTROLLER
A GROUP OF REGISTERS
REGISTER
OUTPUT DESTINATION DETERMINING UNIT
BIT MANIPULATING UNIT
ALU
CONTINUITY DETECTOR
EXTERNAL CPU
HOST I/F
113
115

FIG. 19

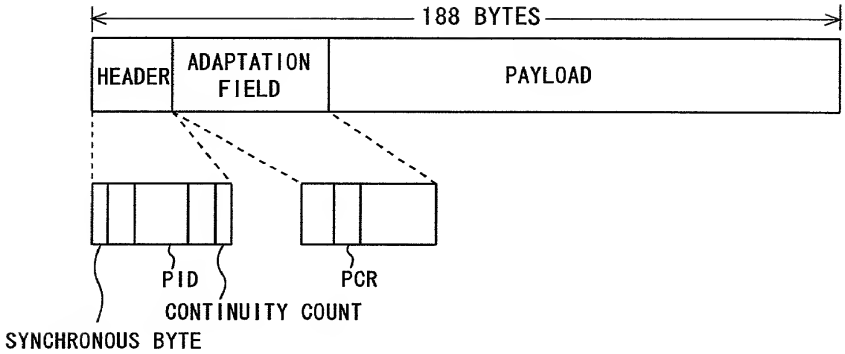


FIG. 20

ITEM	BITS	REMARK
sync_byte	8	IF NOT 0x47, PACKET IS DISCARDED.
transport_error_indicator	1	WHEN '1', PACKET IS DISCARDED.
payload_unit_start_indicator	1	WHEN '1', PES OR PSI HEADER IS CONTAINED.
transport_priority	1	IGNORED
PID	13	COMPARE WITH PID FILTER
transport_scrambling_control	2	WHEN NOT '00', PACKET IS DISCARDED.
adaptation_field_cotrol	2	WHEN '00', PACKET IS DISCARDED. WHEN '10' OR '11', "adaptation_field" IS CONTAINED.
continuity_counter	4	WHEN NOT CONTINUOUS, PACKET IS DISCARDED.

FIG. 21

ITEM	BITS	REMARK
adaptation_field_length	8	length OF "adaptation_field"
discontinuity_indicator	1	IGNORED
ramdom_access_indicator	1	IGNORED
element_stream_indicator	1	IGNORED
PCR_flag	1	WHEN '1', "adaptation_field" CONTAINS PCR.
PCR_base	33	LATCH TO PLL
PCR_extension	9	LATCH TO PLL

FIG. 22

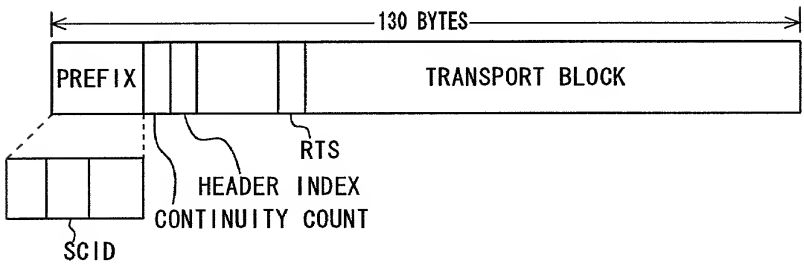


FIG. 23

ITEM	BITS	REMARK
Packet Framing	1	TOGGLE TO '0' OR '1' WHENEVER PACKET IS RECEIVED.
Bundle Boundary	1	IGNIRED
Control Flag	1	WHEN '0', PACKET IS DISCARDED.
Control Sync	1	IGNIRED
Service Channel ID	12	COMPARE WITH PID FILTER.

FIG. 24

ITEM	BITS	REMARK
Continuity Counter	4	WHEN NOT CONTINUOUS, PACKET IS DISCARDED.
Header Designator	4	INDICATES THE TYPE OF VIDEO APPLICATION PACKET.

FIG. 25

ITEM	BITS	REMARK
Modifiable Flag	1	IGNORED
Current Field Flag	1	WHEN '0', PACKET IS DISCARDED.
Aux Field ID	6	INDICATES THE TYPE OF DATA.
Auxiliary Field Size	8	INDICATES THE SIZE OF AUXILIARY DATA BLOCK.

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FIG. 26

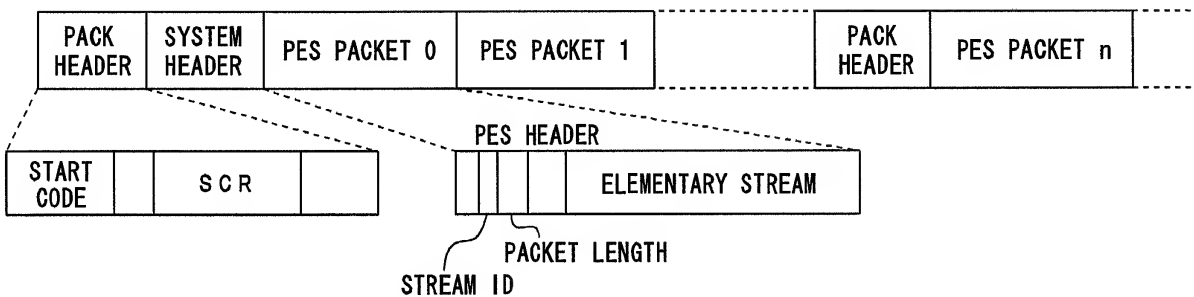

FIG. 27

ITEM	BITS	REMARK
PES_start_code_prefix	24	CARRIES 0x000001
stream_id	8	IDENTIFIES THE TYPE OF ELEMENT STREAM
PES_packet_length	16	INDICATE THE LENGTH OF PES PACKET
PES_header_data_length	8	INDICATE THE LENGTH OF PES HEADER

FIG. 28

ITEM	BITS	REMARK
pack_start_code	32	CARRIES 0x000001BA AS START CODE
syetem_clock_reference_base	33	LATCH TO PLL
system_clock_reference_extension	9	LATCH TO PLL

FIG. 29

ITEM	BITS	REMARK
system_header_start_code	32	CARRIES 0x000001BB AS START CODE
header_length	8	INDICATES THE LENGTH OF SYSTEM HEADER

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FIG. 30

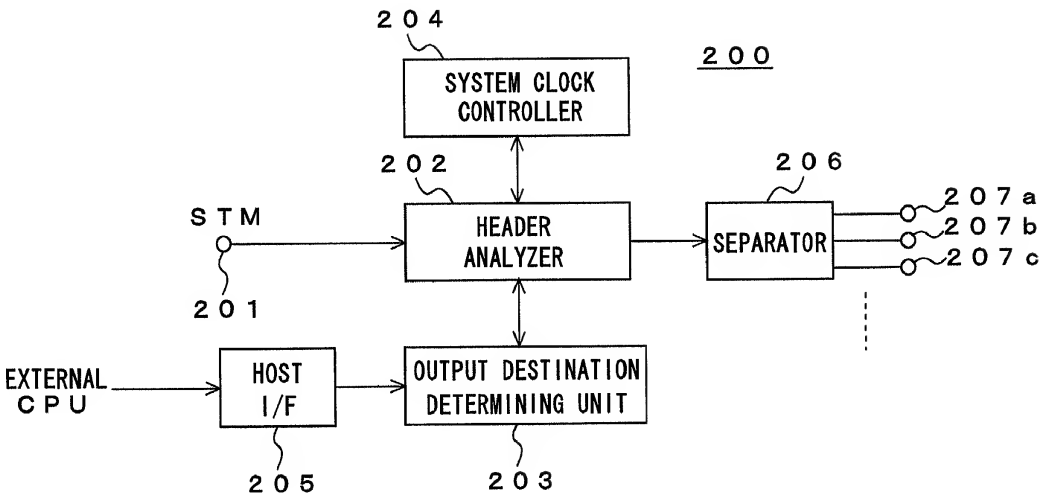


FIG. 31

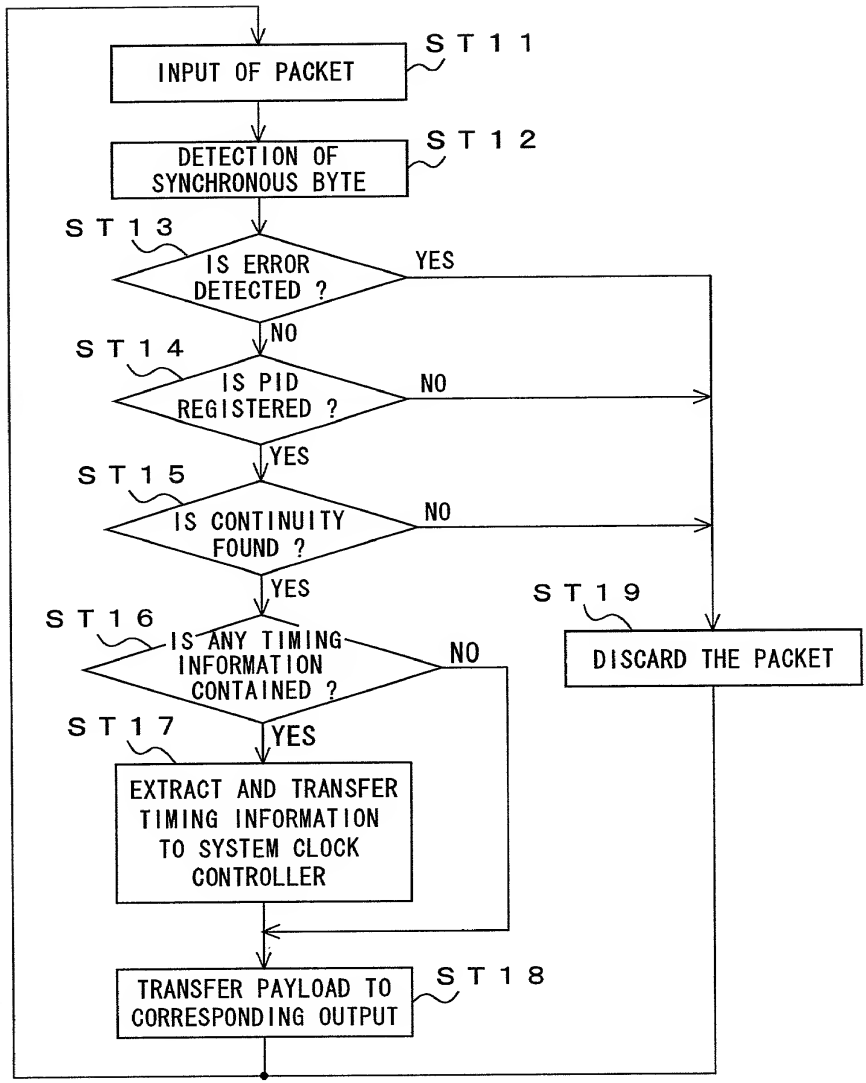

INPUT OF PACKET
ST11
DETECTION OF SYNCHRONOUS BYTE
ST12
ST13
IS ERROR DETECTED ?
YES
NO
ST14
IS PID REGISTERED ?
NO
YES
ST15
IS CONTINUITY FOUND ?
NO
YES
ST16
IS ANY TIMING INFORMATION CONTAINED ?
NO
YES
ST17
EXTRACT AND TRANSFER TIMING INFORMATION TO SYSTEM CLOCK CONTROLLER
TRANSFER PAYLOAD TO CORRESPONDING OUTPUT
ST18
ST19
DISCARD THE PACKET

FIG. 32

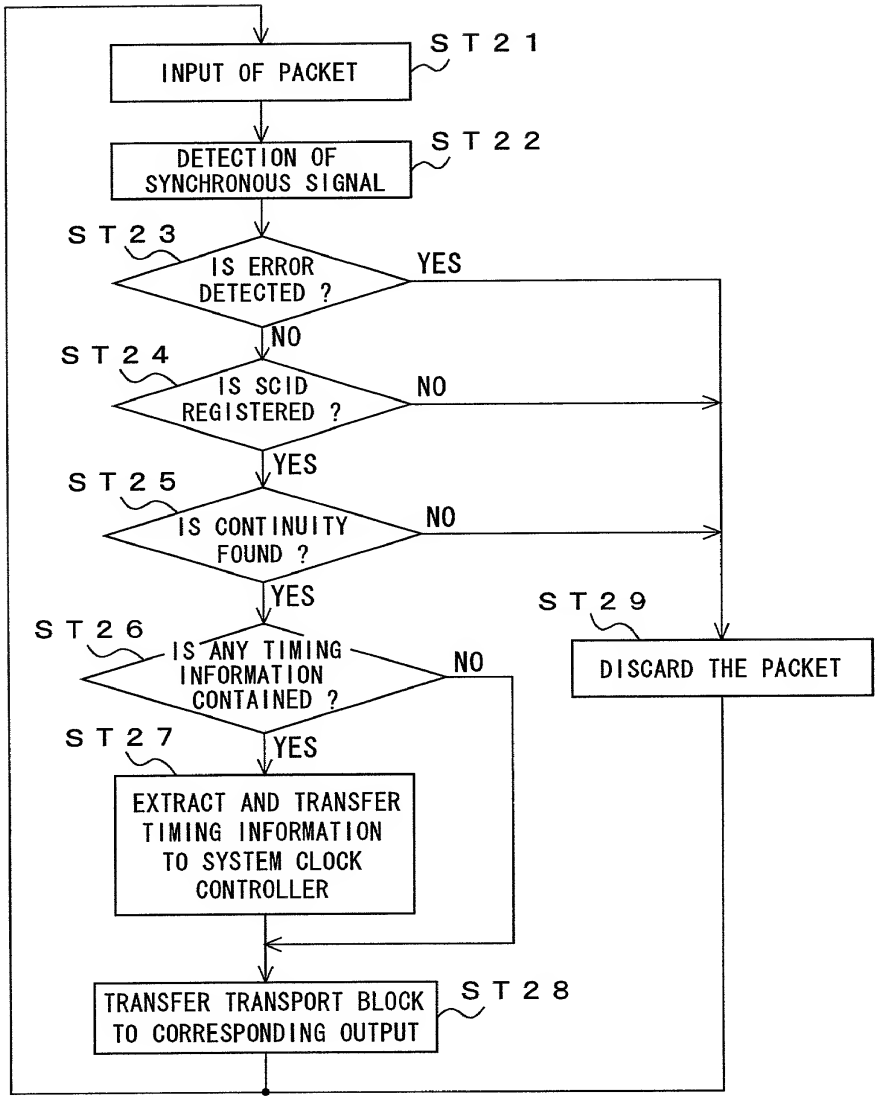
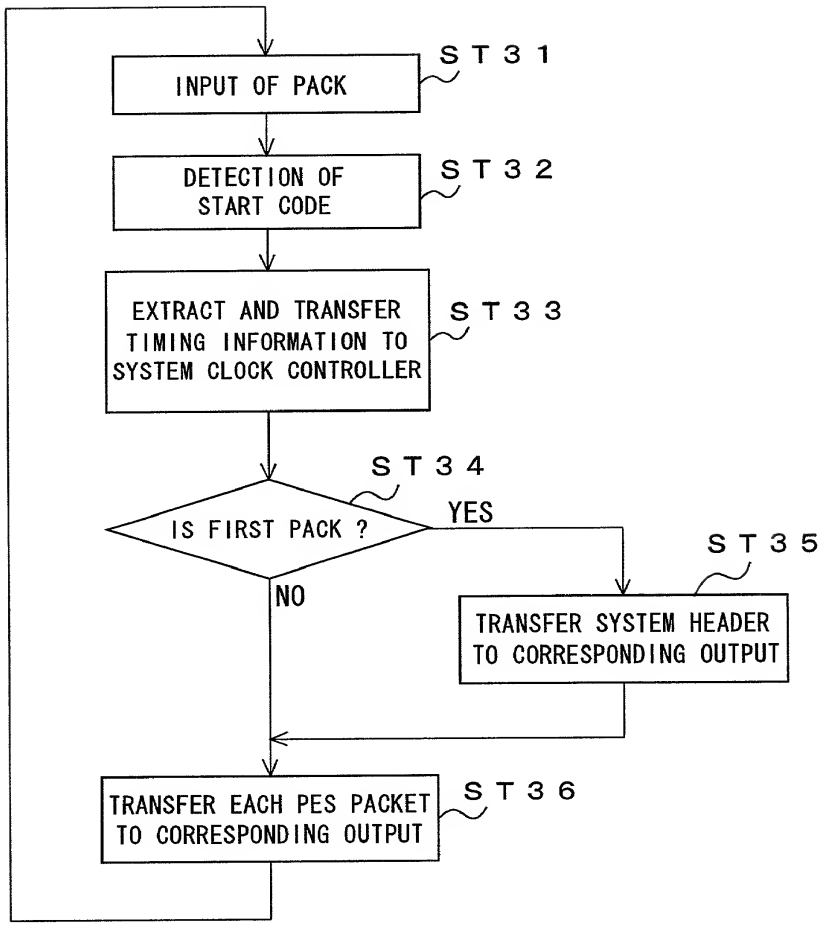

INPUT OF PACKET
ST21
DETECTION OF SYNCHRONOUS SIGNAL
ST22
ST23
IS ERROR DETECTED ?
YES
NO
ST24
IS SCID REGISTERED ?
NO
YES
ST25
IS CONTINUITY FOUND ?
NO
YES
ST26
IS ANY TIMING INFORMATION CONTAINED ?
NO
YES
ST27
EXTRACT AND TRANSFER TIMING INFORMATION TO SYSTEM CLOCK CONTROLLER
TRANSFER TRANSPORT BLOCK TO CORRESPONDING OUTPUT
ST28
ST29
DISCARD THE PACKET

FIG. 33


INPUT OF PACK
ST31
DETECTION OF START CODE
ST32
EXTRACT AND TRANSFER TIMING INFORMATION TO SYSTEM CLOCK CONTROLLER
ST33
ST34
IS FIRST PACK ?
YES
NO
ST35
TRANSFER SYSTEM HEADER TO CORRESPONDING OUTPUT
TRANSFER EACH PES PACKET TO CORRESPONDING OUTPUT
ST36